REMARKS

Claims 1-15 are pending in this application. By this Amendment, claims 13 and 14 are amended. No new matter is added by these amendments. A Request for Continued Examination is enclosed. Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The courtesies extended to Applicant's representative by Examiner Mark Connolly at the interview held March 3, 2008, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below, which constitute Applicant's record of the interview.

The Advisory Action, in paragraph 7, states that the February 19, 2008 Amendment After Final Rejection has been entered but does not place the application in condition for allowance, and the objections and rejections asserted in the November 19, 2007 Final Rejection are maintained.

The November 19, Office Action rejects claims 1, 3, 4, 6-9 and 11-15 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,779,125 to Haban in view of U.S. Patent No. 6,079,024 to Hadjimohammadi et al. (hereinafter "Hadji") in view of U.S. Patent No. 4,980,836 to Carter et al. (hereinafter "Carter"); and rejects claims 1, 3, 4, 6-9 and 11-15 under 35 U.S.C. §103(a) as being unpatentable over Hadji in view of Micron High Performance SDRM Modules (hereinafter "Micron") in view of Carter. Applicant continues to respectfully traverses these rejections.

Specifically, in maintaining the rejections the Advisory Action asserts, *inter alia*, that the Applicant misunderstands the applied reference of U.S. Patent No. 4,980,836 to Carter et al. (hereinafter "Carter"). Applicant respectfully traverses this assertion.

Carter teaches a battery-powered computer system that monitors the address bus to determine when selected peripheral devices have not been accessed for a preset amount of

time. When this preset amount of time has passed, the system powers itself down and stops the system clock, placing the system in standby mode (Abstract). Page 2 of the Advisory Action asserts that Carter teaches that when an access occurs, the timer is restarted so that once the access has completed, the timer can begin to count an inactivity period from anew. This is incorrect. Carter does not teach the timer is started when the access is completed. Instead, in col. 2, lines 15-20, Carter teaches that the system monitors accesses to the hard disk unit, the floppy disk unit, the keyboard, the serial ports and the printer to determine if the system is active. And if so, a timer is restarted on each access. Therefore, Carter teaches that a timer is started when an access is initiated and begins to count down so that if at the end of the countdown period, the system has not been reaccessed, the system shifts into a standby mode. In col. 14, lines 19-27, Carter teaches that generally a sufficient time interval for the timer is considered 70-85 seconds so that the remaining portions of the power-up routine, can be completed. Further, in col. 16, lines 50-53, when shifting into a standby mode, Carter teaches that the system is not immediately made inactive so that the various operations which may be active can be completed. Although not explicitly stated, the entire invention of Carter teaches, or at least would have suggested, that the timer starts at the initiation of the access period and the duration of the timer is of sufficient length to let the current activity complete. This is in direct contrast to the subject matter of the pending claims as discussed below.

Claim 1 recites the first dedicated bus interface block stopping to receive a clock signal a first predetermined time elapsed after an access of the first dedicated bus interface block to the first storage medium is completed. As illustrated in at least Fig. 3, when a storage medium, *i.e.*, SRAM is accessed (52) the clock-supply-control signal for the dedicated bus I/F for the SRAM is terminated when the access to the SRAM is completed, as demonstrated by element 120. Element 80 illustrates that the clock supplied to the dedicated bus I/F for SRAM is terminated thereafter.

The applied references, as enumerated in the November 19, 2007 Office Action of Haban, Hadji and the Micron reference, High Performance with SDRAM Modules, do not overcome the deficiencies of Carter, as discussed above.

For at least the above reasons, the applied prior art references cannot reasonably be considered to teach, or to have suggested, the combinations of all the features recited in at least independent claims 1, 4, 9 and 13. Further, claims 2, 3, 5-8, 10-12, 14 and 15 would also not have been suggested by the applied prior art references for at least the respective dependence of these claims on the allowable independent claims 1, 4, 9 and 13, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejections of claims 1-15 under 35 U.S.C. §103(a) as being unpatentable over the combination of applied prior art references are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-15 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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JAO:KDB/wkb

Attachment:
Request for Continued Examination
Petition for Extension of Time

Date: April 18, 2008

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